CLAIMS

1. A method for making an integrated circuit, comprising:

providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;

providing a first circuit design;

providing an equation which comprises a plurality of variables and constants, wherein the plurality constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;

applying the circuit simulator to the first circuit design to derive a first set of constants for the plurality of constants; and

replacing the unknown constants with the first set of constants to obtain a performance model of the first circuit design;

running experiments using the performance model of the first circuit design;

changing the first circuit design to obtain a second circuit design; and

making an integrated circuit comprising the second circuit design.

2. The method of claim 1, further comprising:

applying the circuit simulator to the second circuit design to derive a second set of constants for the plurality of constants; and

replacing the first set of constants with the second set of constants to obtain a performance model of the second circuit design; and

running experiments using the performance model of the second circuit design.

3. The method of claim 1 wherein the plurality of variables are related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature.

4. The method of claim 1, wherein the equation comprises a plurality of delay expressions.

5. The method of claim 4, wherein the delay expressions comprise:

a metallization resistance and metallization capacitance delay.

6. The method of claim 4, wherein the delay expressions comprise:

a metallization resistance and load capacitance delay.

7. The method of claim 4, wherein the delay expressions comprise:

a transistor impedance and metallization capacitance delay.

8. The method of claim 4, wherein the delay expressions comprise:

an input edge rate and metallization capacitance delay.

9. The method of claim 4, wherein the delay expressions comprise:

a transistor performance as a function of process technology and power supply voltage delay.

10. The method of claim 4, wherein the delay expressions comprise:

a transistor performance as a function of process delay.

11. The method of claim 4, wherein the delay expressions comprise:

a power supply voltage dependent delay.

12. The method of claim 4, wherein the delay expressions comprise:

a temperature dependent delay.

13. The method of claim 1, wherein the equation comprises a plurality of capacitance expressions.

14. The method of claim 13, wherein the capacitance expressions comprise:

a transistor process technology dependent capacitance.

15. The method of claim 13, wherein the capacitance expressions comprise:

a power supply voltage dependent capacitance.

16. The method of claim 13, wherein the capacitance expressions comprise:
a temperature dependent capacitance.

17. The method of claim 13, wherein the capacitance expressions comprise:
a metallization capacitance dependent capacitance.

18. The method of claim 13, wherein the capacitance expressions comprise:
a metallization resistance dependent capacitance.

19. The method of claim 13, wherein the capacitance expressions comprise:
an output load dependent capacitance.

20. The method of claim 13, wherein the capacitance expressions comprise:
an input edge rate dependent capacitance.

21. The method of claim 13, wherein the capacitance expressions comprise:
a power supply voltage and transistor process technology dependent capacitance.

22. The method of claim 13, wherein the capacitance expressions comprise:
a power supply voltage and temperature dependent capacitance.

23. The method of claim 13, wherein the capacitance expressions comprise:

a transistor process technology and temperature dependent capacitance.

24. The method of claim 13, wherein the capacitance expressions comprise: a power supply voltage, transistor process technology, and temperature dependent capacitance.

25. The method of claim 1, wherein the equation comprises a plurality of setup/hold time expressions.

26. The method of claim 25, wherein setup/hold time expressions comprise: an input edge rate dependent setup/hold time.

27. The method of claim 25, wherein setup/hold time expressions comprise: a reference signal input edge rate dependent setup/hold time.

28. The method of claim 25, wherein setup/hold time expressions comprise: a transistor process technology dependent setup/hold time.

29. The method of claim 25, wherein setup/hold time expressions comprise: a power supply voltage dependent setup/hold time.

30. The method of claim 25, wherein setup/hold time expressions comprise: a temperature dependent setup/hold time.

31. The method of claim 25, wherein setup/hold time expressions comprise:

a metallization resistance dependent setup/hold time.

32. The method of claim 25, wherein setup/hold time expressions comprise: a metallization capacitance dependent setup/hold time.

33. The method of claim 25, wherein setup/hold time expressions comprise: an output load dependent setup/hold time.

34. The method of claim 25, wherein setup/hold time expressions comprise: a transistor process technology and power supply voltage dependent setup/hold time.

35. The method of claim 25, wherein setup/hold time expressions comprise: a metallization resistance and a metallization capacitance dependent setup/hold time.

36. A machine readable medium have stored therein information comprising:

an equation which comprises a plurality of variables and constants, wherein the plurality constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature; and

means for replacing the unknown constants with the first set of constants to obtain a performance model of the first circuit design.

37. A method for obtaining a performance model, comprising:

providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;

providing a path comprising a first design block, a second design block, and an interconnect coupling the first design block to the second design block;

providing an equation which comprises a plurality of variables and constants, wherein the plurality constants are unknown constants and one of the variables is related to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature;

applying the circuit simulator to the first and second design blocks to derive a first and second set of constants for the plurality of constants;

replacing the unknown constants with the first set of constants to obtain a first performance model of the first design block and the second set of constants to obtain a second performance model of the second design block;

modeling the path using the first performance model and the second model;

changing the design of at least one of the interconnect, the first design block, and the second design block to obtain a revised path; and

making an integrated circuit comprising the revised path.